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INTENSITY THRESHOLD STUDY OF 6T, 7T AND 10T SRAM BY TCAD SIMULATION WITH OPTICAL BEAM

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ABSTRACT

Due to hazard and difficulty of emulating high energy space particle and rays in labs, Technology Computer Aided Design (TCAD) simulation is considered as a viable alternative for any space exploration. This paper presents a TCAD simulation to show a comparison study of intensity threshold for 6-T, 7-T and 10-T SRAM. To show the comparison, Single Event Upset (SEU) simulation has done with pulsed optical beam by mixed-mode feature of Silvaco ATLAS. Mixed- mode is a mixed circuit and device simulator which can handle both circuit and device. In this study, SRAM cell have been simulated by using SPICE coding in mixed-mode where targeted transistor is a physically based device. The target transistor is used to evaluate the intensity threshold for bit-flip in the simulated SRAM circuit. This method significantly reduce the time of simulation and can handle both the device and circuit simultaneously. The results show that for these particular structures, intensity threshold is increasing with the increase of transistor number in the SRAM. This study shows a new feature of larger transistors SRAM though it has some area penalty.

Keywords: Mixed-mode simulation; Optical beam; Intensity threshold; Single Event Upset (SEU); SRAM, Bit-flip;

INTRODUCTION

According to "Moor's Law" observation, in a dense integrated circuit, the number of transistors has doubled approximately in every two year [1]. This is referring to the miniaturization of devices and transistors. When the device become smaller, their capacitance also reduced. According to charge capacitance direct relationship equation, if the capacitor is reduced, smaller number of charge can be stored in the device. This phenomena increases the probability of occurring ionizing radiation [2]. In semiconductor perspective, ionizing radiation refers to a phenomena where highly energetic particle or ray transfer its energy to a material which causes the generation of electron-hole pair. These free electron hole pair causes extra current and change the characteristic of the device. Particularly electronic device like memory cell are more

vulnerable to these ionizing radiation. Especially in space where there is huge number of highly energetic particle exist, the chance of cell damaging or data loss of a memory cell due to ionizing radiation is highly increased. In the past few years, Single Event Effect (SEE) is the most observed ionizing radiation in the space [3], single event upset (SEU) is one of its kind which mainly found in the memory cell. This is due to the device miniaturization trend discussed previously. SEE is mainly divided into three categories: (i) Single Event Upset (SEU); (ii) Single Event Burnout (SEB); and (iii) Single Event Latchup (SEL). Details explanation on all these events can be found in [4, 5, 6]. This research is only focused on SEU.

Some recent papers gives experimental and theoretical results that showed SEU can occur by using a monochromatic beam, laser and many more optical sources [7, 8, 9]. According to recent studies, SEU has devastating effect on electronic devices specially memory cell like SRAM. SEU change the memory of an SRAM and sometimes it can damage the entire cell. Due to these problem there are many ongoing research on SEU effect on SRAM but most of them addressed the basic 6 T SRAM structure. Research on SEU with optical beam is still infancy. In order to address these question we perform a comparative study of SEU effect on 6 T, 7 T and 10 T SRAM with optical beam of different intensity.

EXPERIMENTAL

Simulation Details

High energy space particles and rays are potentially hazardous to microelectronic circuits and systems. Among the electronic circuits, used in space exploration, SRAM has the worse radiation effect. High energetic space particles and rays can cause bit flipping in an SRAM and change the memory of it. Due to this devastating radiation effect literature review shows, there are many research about SEU effect on SRAM, though none has done the comparative radiation effect on different types of SRAM. In this research we studied SEU effect on different types of SRAMs such as 6 T, 7 T and 10 T SRAM. Figure 1 shows the structure of 10 T SRAM.

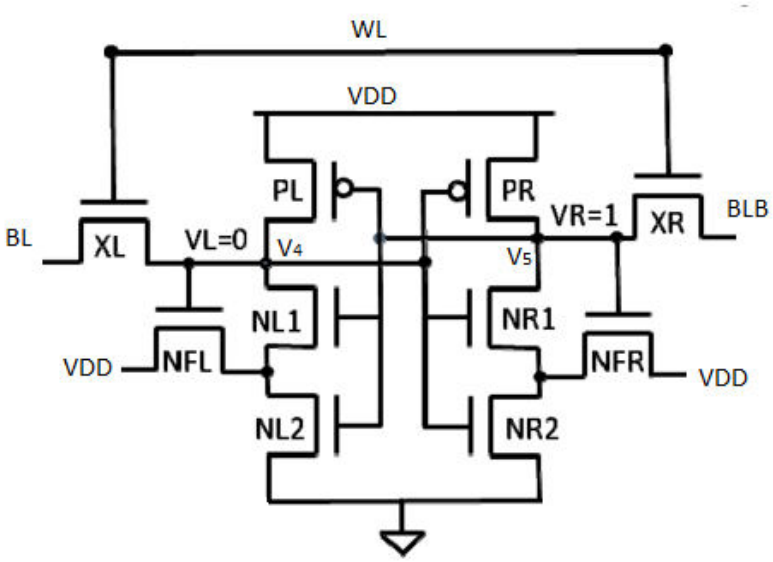


Figure 1: Structure of 10 T SRAM [10]

10-T SRAM structure used in the research is shown in figure 1. In this structure, there are two PMOS and eight NMOS transistors. PL and PR are two PMOS pull-up transistors and the other four NMOS (NL1, NL2, NR1, and NR2) are pull-down transistors. There are also two NMOS access transistors (XL and XR) in the structure. By these access transistor bit (BL) and bit-bar (BLB) line are connected to the main memory cell. Access transistors are operated by word line. To turn on the access transistors word line must be high. When the word line is high and access transistors are on, BL and BLB lines are connected to the memory cell. On the other hand, when the word line is low and access transistors are off, BL and BLB lines are not connected with memory cell. The width and length of the transistor are taken as follows: the W/L of the P-channel transistors of these SRAMs is 0.8/0.45 um, the W/L of the N-channel transistors is 0.8/0.35 um, and the W/L of the N-channel access transistors is 1.0/0.35 um.

In this simulation all optical beam is rectangular and strike at an angle of 90 degree which means it strike direct perpendicularly to the device and it creates a radial path of electron/hole pairs. From now on through this paper optical beam is named as beam only.

RESULTS AND DISCUSSION

Sensitive Striking Position of Device.
Different amount of electron-hole pair is generated for striking different position in the device. As the number of carrier is different for striking different position, the amount of current is also different. Previous papers reported that, off-state NMOS drain is the most sensitive strike position for bulk CMOS technologies [11, 12]. Even in drain area different amount of carrier has generated when beam strike in the edge of drain and in

the middle of drain. In this study current has been measured when beam striking different position of the device. Fig 2 shows that, when beam strike at the middle of drain highest amount of current generated and this is one of the most sensitive node of an off NMOS transistor for SRAM. In this simulation, different position has been chosen but all beam strike at an angle of 90 degree which means it strike direct perpendicularly to the device and it creates a radial path of electron/hole pairs.

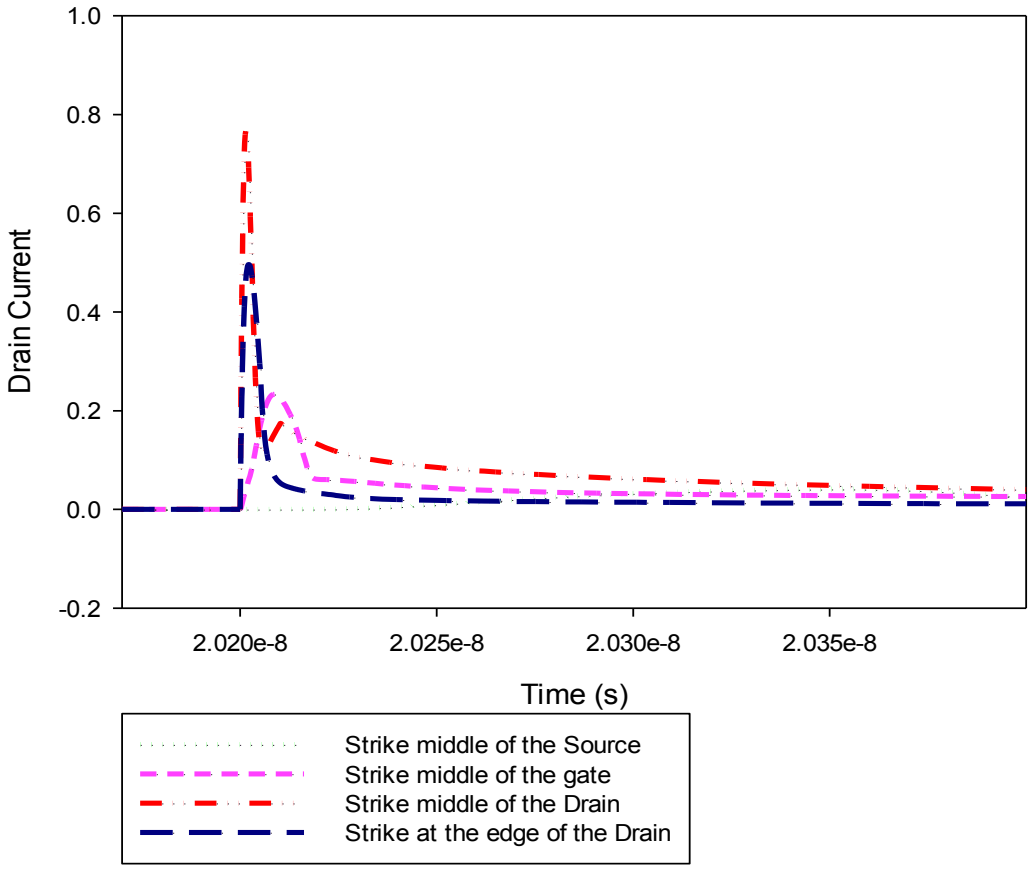


Figure 2: Drain Current when Beam strike different position of the device

In this study the beam strike exactly at 20 ns. At this point when the beam strikes, a huge number of carrier generated. Compare to this amount of carrier, previous amount of carrier (before beam strike) is almost negligible. For this reason, in figure 1, current before 20 ns is almost zero compare to the current after 20 ns. Another observation is the peak of current found just after the strike, which actually causes the data loss or memory flip. After 20 ns, current reduces gradually with passing of time.

Intensity Threshold Study.

High energetic space particles and rays can cause bit flipping in an SRAM and change the memory of it. When any space rays or particle strike an electronic device, huge

number of electron-hole pair generated. In Silvaco Atlas, the electron-hole pair generation is calculated by Eq. 1 for photo-generation TCAD model (this is the final form of equation, see [13, chapter 10, page 513 and 522] for further details).

$$G = \eta_{\infty}\left(\frac{P\lambda}{hc}\right)\alpha e^{-\alpha y} \quad (1)$$

where *P* is the ray intensity factor, which contains the cumulative effects of reflections, transmissions, and loss due to absorption over the ray path, η_{∞} is the internal quantum efficiency, which represents the number of carrier pairs generated per photon observed, *y* is a relative distance for the ray in question, *h* is Planck's constant, λ is the wavelength, c is the speed of light, α is the absorption coefficient given by Eq. 2,

$$\alpha = \frac{4\pi}{\lambda}k \quad (2)$$

where *k* is the imaginary part of the optical index of refraction.
In ATLAS framework, intensity profiles along with light propagation and absorption program are converted into photo-generation rates, which are directly integrated into the generation terms in the carrier continuity equations.

Figure 3 shows the intensity threshold point for 10 T SRAM. Intensity threshold point is determined by the minimum intensity where upset measured. In this study beam strike at 20 ns. When the beam strikes at 20 ns, a huge number of carrier is generated. This extra carrier creates a peak of current which actually flip the bit and reverse the data. In figure 3, for $1.17\text{x}10^{8}$ W/cm^2 the bit is flipped whereas for $1.16\text{x}10^{8}$ W/cm^2 there is no flipping. So, the intensity threshold point for 10 T SRAM is $1.17\text{x}10^{8}$ W/cm^2. For 6 T SRAM we found upset at $1.08\text{x}10^{7}$ W/cm^2 whereas for $1.07\text{x}10^{7}$ W/cm^2 there is no upset. So, the intensity threshold point for 6 T SRAM is $1.08\text{x}10^{8}$ W/cm^2. For both 6 T and 10 T there are no overlapping of voltage level before flipping. There has an interesting observation for 7 T SRAM. In 7 T SRAM there are overlapping of two voltage level even before flipping which is shown in figure 4.

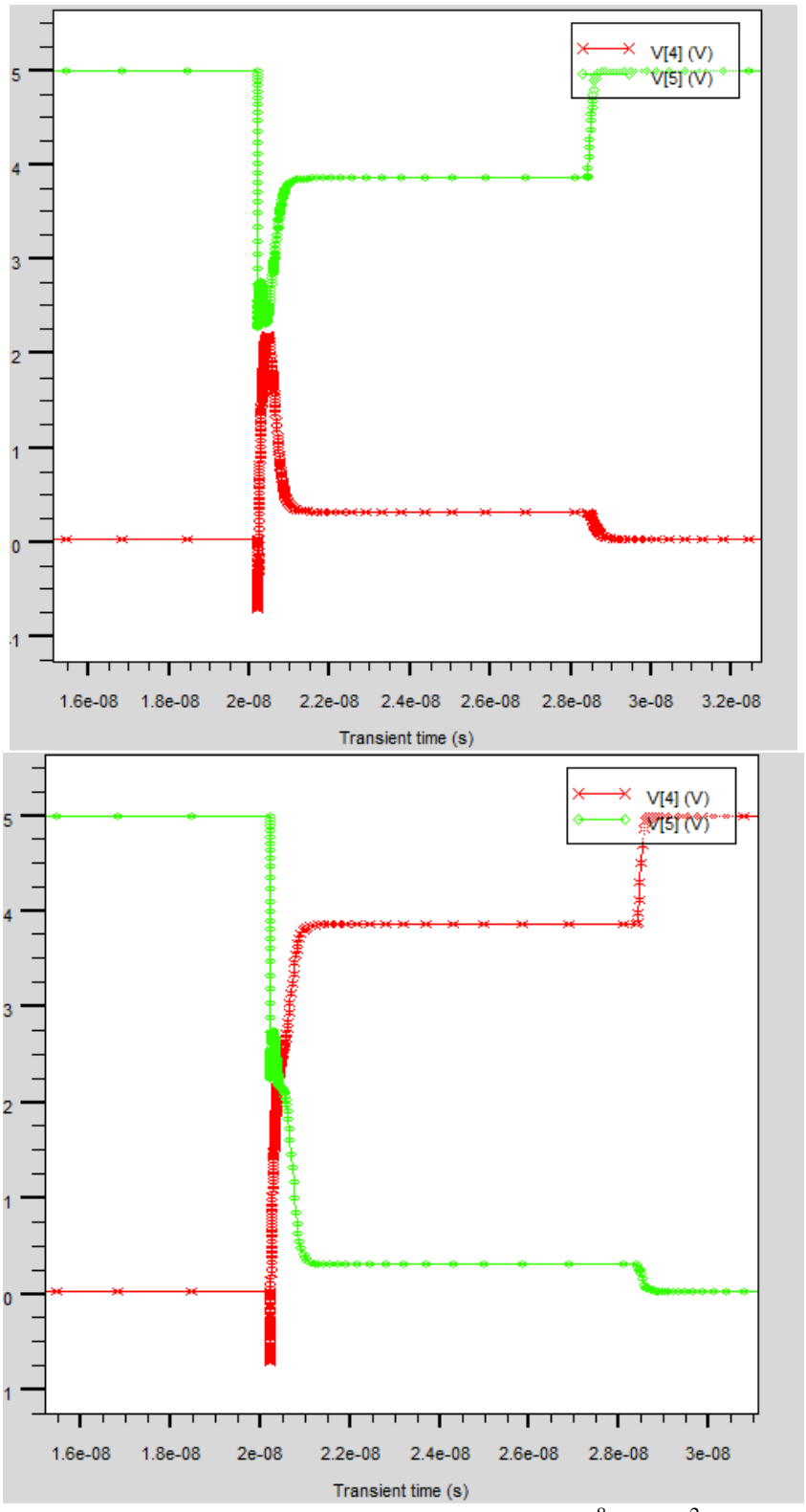


Figure 3: Output of 10T SRAM with intensity of 1.16×10^8 W/cm^2 (left) and 1.17×10^8 W/cm^2 (right)

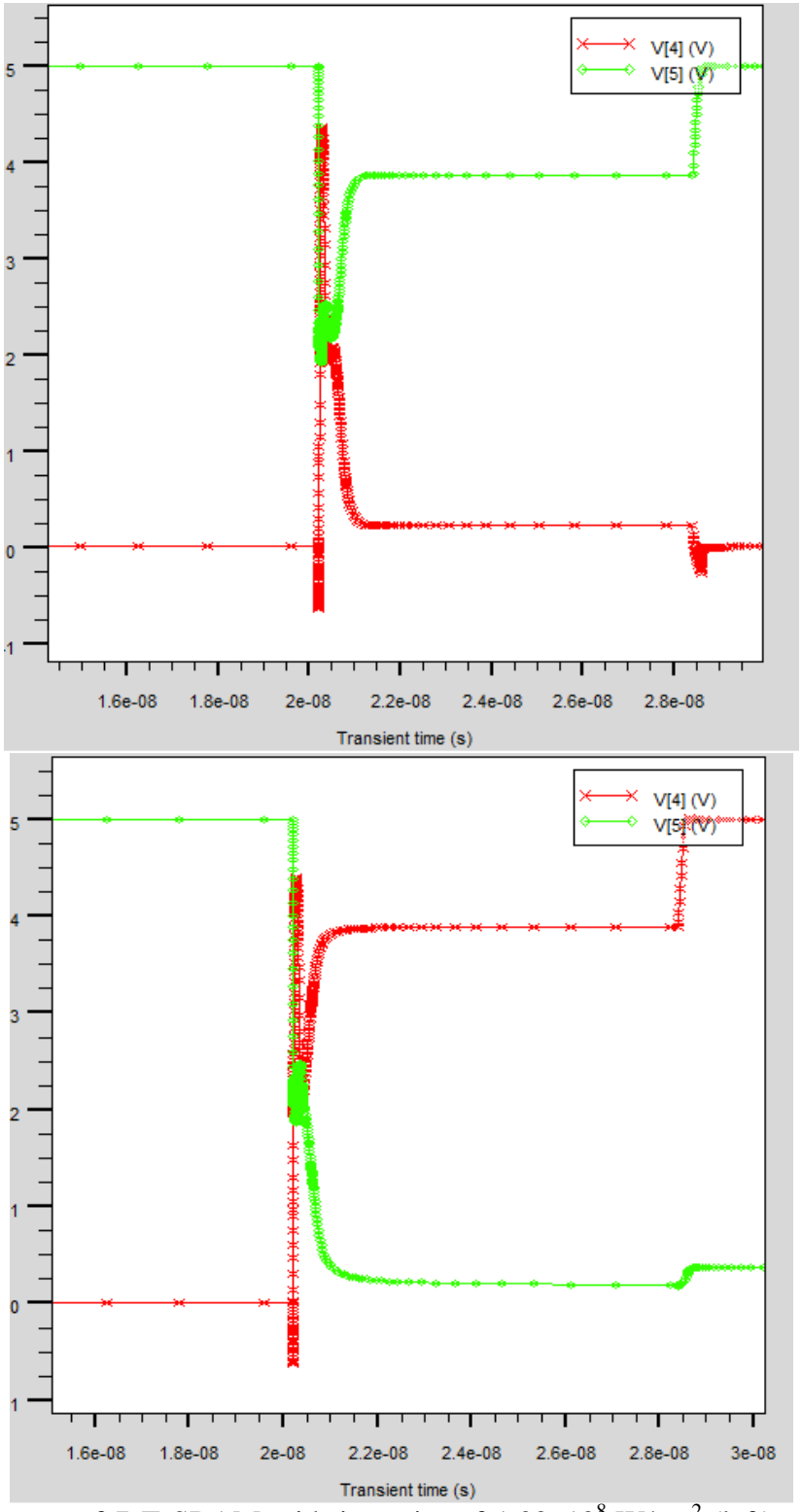
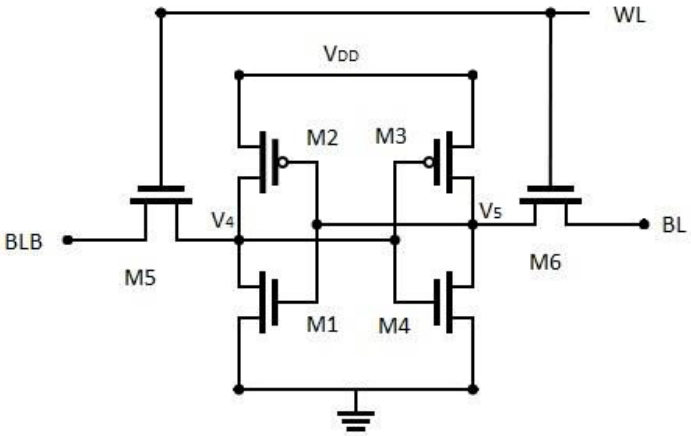
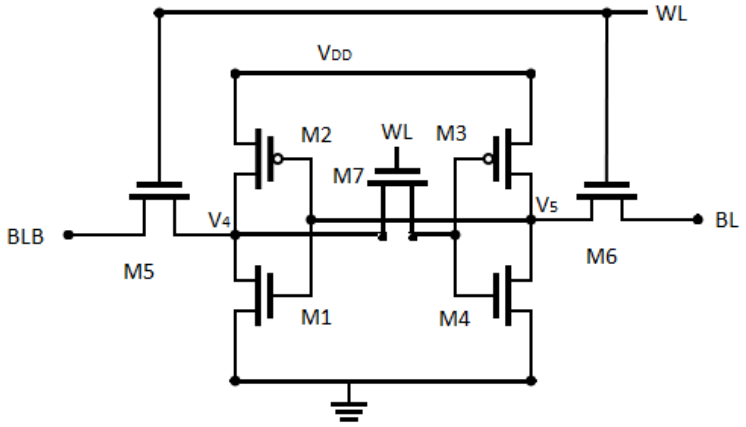


Figure 4: Output of 7 T SRAM with intensity of 1.03×10^8 W/cm^2 (left) and 1.04×10^8 W/cm^2 (right)

Figure 4 shows the intensity threshold point for 7 T SRAM. In this case we found upset at $1.04x10^8$ W/cm^2. So the intensity threshold point for 7 T SRAM is $1.04x10^8$ W/cm^2. The interesting fact is at $1.03x10^8$ W/cm^2 we don't found upset but there are overlapping of voltage level. This is because the structure of 7 T SRAM which is shown in figure 5. In 7 T SRAM there is an extra NMOS in the main memory cell which is situated in between node 4 and node 5. For this extra NMOS transistor the self-recovery time increases. As a result though there is more carrier generated but upset didn't occurs. This type of conditions also reported in some other paper. Sometime more charge in the sensitive node didn't cause upset whereas less charge causes upset [14]. This is mainly because of the structure of the cell and depending on the feedback path of the cell.



(a)



(b)

Figure 4: Structure of 6 T SRAM (a) and 7 T SRAM [15] (b)

CONCLUSION

In this mixed-mode simulation, beams of different intensity strike SRAMs and we measure the intensity threshold point for 6-T, 7-T and 10-T SRAM. Among these SRAMs, 10-T induces more radiation hard SRAM whereas 6-T is the least radiation hard. Most sensitive place for beam strike is also discussed in this paper. A TCAD software Atlas, SILVACO has been used to do all these simulation.

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