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O_2 PLASMA BASED SIZE REDUCTION FOR NANO ELECTRONICS DEVICE FABRICATION

Th. S. Dhahi[1,*], U. Hashim[1], N. M. Ahmed[2] and A. Mat Taib[1]

[1]*Institute of Nano Electronic Engineering,*
University Malaysia Perlis (UniMAP)
Lot 106, 108 & 110, Tingkat 1 Block A, Taman Pertiwi Indah,
Jalan Kangar-Alor Setar, Seriab, 01000 Kangar, Perlis, Malaysia

[2]*School of Micro Electronic Engineering, (UniMAP)*
Block A, Kompleks Pusat Pengajian KUKUM,
Northern Malaysia University College of Engineering,
02600 Jejawi, Perlis, Malaysia

ABSTRACT

The field of plasma chemistry has provided some understanding of plasma processes. By controlling plasma conditions and gas mixtures, ultra-fast plasma cleaning and etching is possible. Plasma has frequently been used by the industry as a last step surface preparation technique in an otherwise predominant wet-etched process. With enhanced organic removal rate, plasma processes become more desirable as an environmentally sound alternative to traditional solvent or acid dominated process, not only as a cleaning tool, but also as a patterning and machining tool. In this paper, photoresist (PR) stripping using O_2 plasma process in nanogap fabrication is explained including many parameters for PR patterning with limited time in O_2 plasma process. And the applications that have not been possible with limited usefulness, plasma processes are now approaching the realm of possibility. We introduce this proposal to fabricate the nanogap device using O_2 plasma technique as a size reduction for biosensor fabrication. In this review, the 2 masks designs are proposed. The first mask is for the lateral nanogap and the second mask is for a gold pad electrode pattern, and lateral nanogap is introduced in the fabrication process using polysilicon, and gold as an electrode. Conventional photolithography technique is used to fabricate this nanogap (NG) based on the plasma etching technique.

Keywords: O_2 plasma; nanogap;

INTRODUCTION

Whereas it has long been recognized that atoms and radicals are far more chemically reactive than most molecules, this principle was not extensively utilized in the etching of solids until the early 1960's when small oxygen plasma systems became available for the removal of carbonaceous residues [1]. This technique was soon extended to the

etching of silicon and its compounds with fluorine and chlorine-containing gases [2]. The early systems that became available during this period were the so-called "barrel" systems in which the surfaces to be etched are immersed in the plasma without any electrical bias applied. That is, the surfaces are at the floating potential of the glow discharge and would be subjected to only low-energy (~<30 eV) ion bombardment in most discharge configurations. In addition, in some situations, the surfaces to be etched were isolated from the glow discharge by a cylindrical metal mesh (etched tunnel) [3] and, in this configuration, no energetic charged-particle bombardment of the surfaces would be expected. The etching which takes place in such an environment is primarily isotropic (see Figure1) [4].

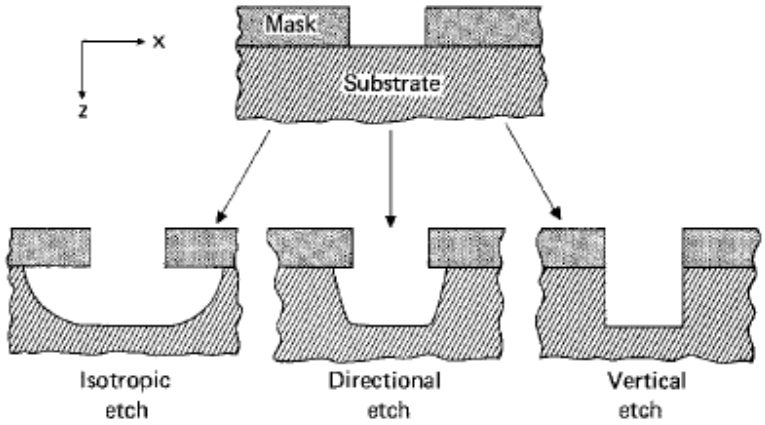

Figure1: Directionality of etching processes

Although there are numerous instances in which isotropic plasma etching can be used effectively, the most valuable aspect of the plasma-assisted etching technology is the ability to etch in a highly directional manner. It was not until several years later that the directional etching was obtained when the etched surfaces were subjected to energetic ion bombardment (usually a few hundred eV) beginning to be recognized and used in microstructure fabrication [5, 6]

Advanced semiconductor integrated circuit device chips are typically manufactured through processes which provide multiple conductive layers and multiple insulating layers upon a plurality of active semiconductor substrate regions. These layers and regions are typically defined and formed through etching and masking processes which involve the photolithographic exposure and developing of blanket photoresist layers. Commonly, a photolithographically exposed blanket photoresist layer will be developed into a patterned photoresist layer through which features, to be formed within or upon a semiconductor substrate, are defined.

Subsequent to photolithographic exposure and development, patterned photoresist layers which remain upon a semiconductor substrate may be exposed to semiconductor manufacturing processes which significantly alter the chemical or physical structure of those patterned photoresist layers. Such manufacturing processes may include: (1)

implanting of high doses of dopant species into those patterned photoresist layers, (2) exposure of those patterned photoresist layers to substantial quantities of radiative energy, or (3) exposure of those patterned photoresist layers to elevated temperatures. Each of these manufacturing processes may produce changes in patterned photoresist layers which yield substantial concentrations of oxidized species within those patterned photoresist layers.

Typically, patterned photoresist layers are removed prior to forming over-lying layers of the semiconductor structure within which those patterned photoresist layers were formed. Commonly, patterned photoresist layers are removed from the semiconductor substrates upon which they were formed through exposure of the patterned photoresist layers to the oxygen Reactive Ion Etch (RIE) plasma. However, patterned photoresist layers which contain substantial quantities of oxidized species may be difficult to be removed from semiconductor substrates through the oxygen Reactive Ion Etch (RIE) plasma processes since oxidized species within patterned photoresist layers are often unaffected by the chemical and physical effects of the oxygen Reactive Ion Etch (RIE) plasma. Thus, it is often necessary to include into such oxygen Reactive Ion Etch (RIE) plasma a reducing material which may react effectively with the oxidized species contained within the oxidized patterned photoresist layer.

The most common reducing material which may be incorporated into the oxygen Reactive Ion Etch (RIE) plasma to assist in removal of oxidized species within patterned photoresist layers is hydrogen gas. The hydrogen gas is typically incorporated into the oxygen Reactive Ion Etch (RIE) plasma in the form of gas mixtures such as nitrogen/hydrogen and helium/hydrogen mixtures. While the oxygen Reactive Ion Etch (RIE) processes which contain reducing materials such as the hydrogen gas are usually quite effective in removing oxidized organic residues such as oxidized photoresist residues from semiconductor substrates, such Reactive Ion Etch (RIE) plasma is not free from the problems.

In particular the hydrogen gas containing reducing materials when used within the oxygen Reactive Ion Etch (RIE) plasma is typically expensive in comparison with other materials used within the Reactive Ion Etch (RIE) plasma. In addition, the hydrogen gas mixtures when provided into the oxygen Reactive Ion Etch (RIE) plasma also possess an inherent safety concern which is related to the explosive characteristics of the hydrogen gas in ambient atmospheres which contain oxygen. Therefore, although it is desirable to provide the oxygen Reactive Ion Etch (RIE) plasma containing a sufficient quantity of reducing material to effectively remove oxidized organic residues such as oxidized photoresist residues from the semiconductor substrates, it is also desirable that the reducing material incorporated into that oxygen Reactive Ion Etch (RIE) plasma produces plasma which is both economical and safe to be used in a manufacturing environment. It is towards these two goals that the present invention is directed [7].The mechanistic and parametric complexity of the plasma etching environment often causes confusion and delays in the development of a suitable plasma etching process. Plasma pressure may be one of the most important process parameters.

In systems where the primary mechanism of plasma etched is the chemical etching component, increased pressure in the chamber results in more reactive species present. In system in which ion bombardment is the primary actor, an increase in pressure does not have such a pronounced effect although system pressure can affect ion density and energy. For example in etching the Si in aCF_4/O_2 plasma, in a low pressure regime, ion bombardment is the dominant player and the result is an anisotropic etched. At higher pressures, neutrals play an important role and chemical etching enhances etch rate resulting in a more isotropic etch [8].The pressure of the system also impacts the dc self-bias. In a reactive ion etch system, the increased pressure will reduce dc self-bias. At lower pressures, electron temperature will increase and result in an increase in dc bias. Therefore, the etch rate of ion-enhanced processes could be reduced with increasing pressure [9]. In higher pressure systems, lower peak to peak voltages are required which result in lower average ion energies [10]. Lower pressures result in higher energy and less off-axis ion bombardment. In other words, as pressure increases, ion flux increases but ion energy decreases. As pressure decreases, ion fluxes decreases and ion energy increases [11].

EXPERIMENTAL DETAILS

In this project, the Si wafer is used as a starting material to fabricate the nanogap biosensor. The first step is to fabricate two designs as two masks, in which the two mask design is proposed and the polysilicon nanogap with the gold electrode process flow is designed. This Research mainly focuses on the issue related to the fabrication of the biosensor and the development of a new technology.The sidewall etching using the O_2 plasma (RIE) to form thin polysilicon nanogap metal cantilevers which configure the 3-D nanogap electrode grid array structure. The anisotropy of the RIE is modeled and the etching profiles are simulated. This method is proved to be applicable by analysis and experiments [12].

The starting material use in this project is the Si wafer, 100mm in diameter (4 inch wafer). The first process is to check the wafer type from its specification, measure wafers thickness (Si thickness), and measure the sheet resistance . After that, lightly scribe the backside of the wafer and protect the top surface, using the scribing tool provided. Making a gentle but visible mark and then place scribed wafer in a container, the wafer is cleaned before each of the processes. As for the lithography process, two photomasks are employed to fabricate the nanogap using conventional photolithography and O_2 plasma techniques.

A commerical chrome mask is expected to be used in this research for better photomasking process. This mask is used to develop the gold electrode with the polysilicon nanogap. The photomasks are designed via AutoCAD software and then printed onto a chrome glass surface.

Figure 2 is the first mask for the nanogap electrode formation with the length and width of 5000μm and 2500μm, respectively.

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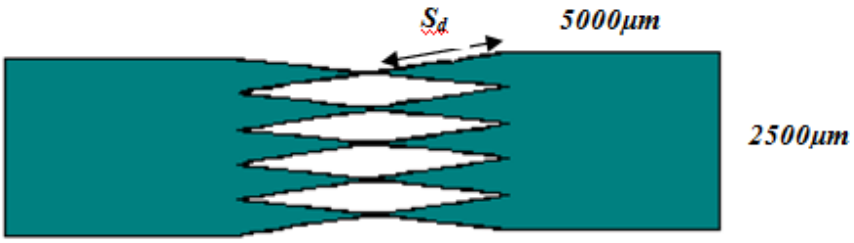

Figure 2: Design Specification of the Mask1

The proposed angle length of the end electrode is shown in Table 1. This is simply to check the best angle for the best nanogap formation after the etching process.

Table 1: Dimensions for S_d.

S_d	μm
1	1100
2	1000
3	900
4	800
5	700
6	600

The symbol S_d refer to the dimension for the Side angle of the design of the nanogap formation. It is shown that when S_d is large the nanogap becomes very sharp and the sharpness decreases with the lesser sharp with less dimension of S_d.
Figure 3 shows the actual arrangement of device design on a chrome mask. It is consists of 160 dies with 6 different designs.

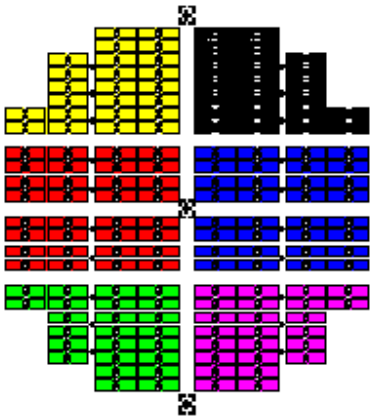

Figure 3: Schematic design of the actual mask on chrome glass

Figure 4 is a schematic device design of Mask 2 with 5000μm long and 2500μm wide.

The distance between the two rectangles is indicated as S_a bearing the same dimension with S_d according to the theorem of Pythagoras, and the dimension of S_a can be defined mathematically as shown in Figure 5.

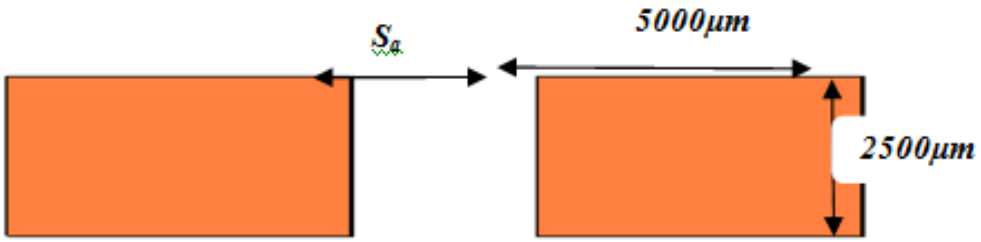

Figure 4: Design Specification for Mask 2

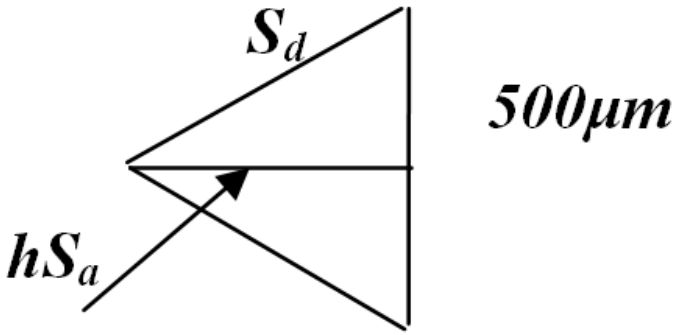

Figure 5: Schematic representation S_a, where $S_a=2hS_a$

Table 2: Variance Dimensions for S_a verses the Dimension for S_d.

S_d (µm)	$hS_a=((S_d)^2-(250)^2)^{1/2}$ (µm)	$S_a=2\ hS_a$ (µm)
1100	1071	2139
1000	968	1936
900	864	1729
800	759	1519
700	653	1307
600	545	1090

From the above table the dimension for S_a depends on the dimension of S_d ,. The calculated S_a is based on $S_a=2hS_a$. Figure 7 is a schematic mask on a chrome glass.

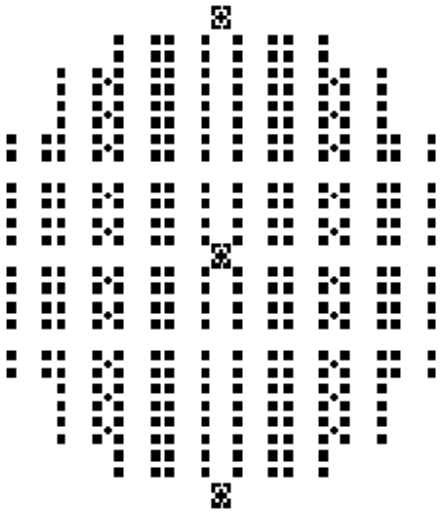

Figure 6: Schematic mask on chrome glass

Nano Electronic Device Fabrication

We start the process steps polysilicon nanogap fabrication with gold electrodes, by cleaning the Si wafer and then deposit polysilicon layer over the Si wafer before depositing 135nm of Al as a hard mask to avoid damage of the polysilicon layer during etching, by using the RIE. In order to optimize the photoresist (PR) patterning using O_2 Plasma stripping in nano electronic device, the Si wafer must be cut after Al deposit process to four pieces where the applied PR different as shown in the Table 3.

Table 3: various parameters for PR process

No. Sample	Step 1 for PR	Step 2 for PR
1	rpm=600	rpm=4000
2	rpm=600	rpm=3000
3	rpm=800	rpm=4000
4	rpm=800	rpm=3000

After the PR coating, we use the same group of samples from Mask1 for all the samples (Si/polySi/Al/PR wafer), and develop the resist before hard mask process, then apply the wet etching for Al layer (Figure 7).

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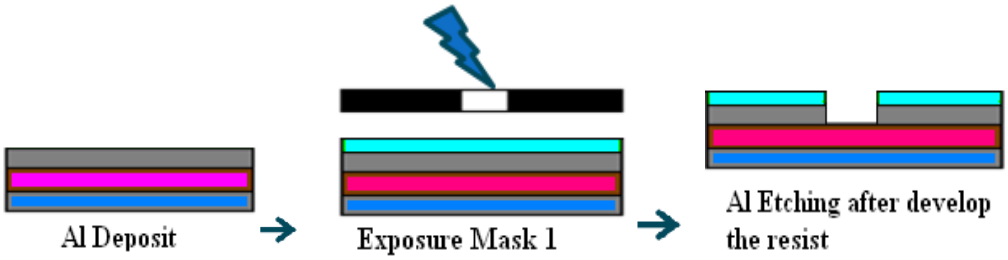

Figure 7: The first steps for nano electronic device fabrication

Formation of the nanogap is aided by O_2 plasma technology, which we mentioned in the introduction and we also use the limited time to take a closer look at the impact of the latest on this technology. Therefore, before the wet etching of the Al layer, it is best to fabricate the gap using the RIE /O2 plasma and the following parameters as in Table 4.

Table 4: Explain the parameters for O_2 plasma process

CF_4	CHF_3	SF_6	O_2	Ar	Bias	Power ICP Power	APC/Control (Pa)
0	0	0	20	0	30	200	1.00

RESULTS AND DISCUSSION

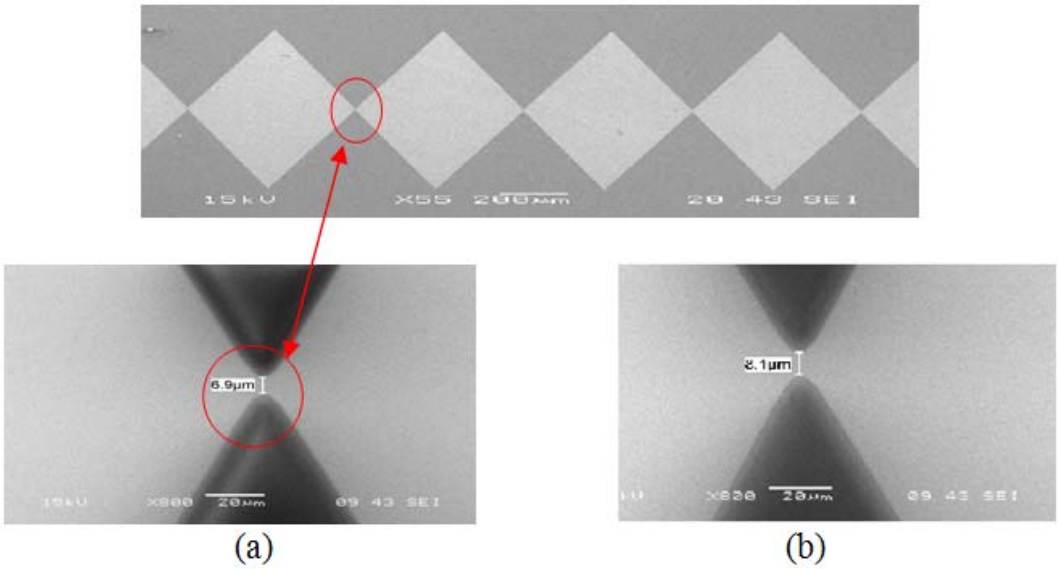

Figure 8: SEM photo show the image gap as 15 kV for sample 1:
(a) Before O_2 plasma the size of the gap is equal to 7.6µm, (b) After O_2 plasma the size of the gap is equal to 7.9µm

Using the parameters of Table 4 for the RIE with a time value of 10 sec. Sample1 and sample2 have produced the following results as shown in Figure 8, where the parameters used in the process of photoresist (PR) in the sample1 is different from that in the sample2, as shown in Table 3. Initial gap size for Sample1 is 7.6µm whereas after O_2 plasma etching the final of the gap size is 7.9µm and the removal of the resist via PR strip increases the size of the gap by 0.3µm as shown in the Figure 9.

The initial gap size for Sample2 is 6.9µm whereas after O_2 plasma etching the final of the gap size is 8.1µm and the removal of the resist increases the size of the gap by 1.2µm as shown in the Figure 9.

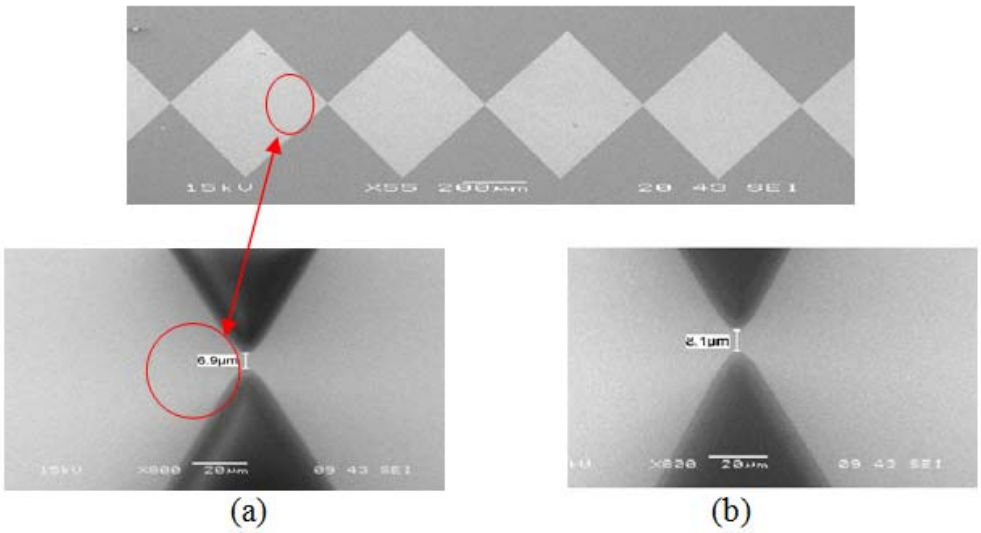

Figure 9: SEM photo show the image gap as 15 kv for sample2:
(a) Before O_2 plasma the size of the gap is 6.9µm, (b) After O_2 plasma the size of the gap is 8.1µm

It appeared clear that the parameters used in the process of photoresist (PR) in Figure 9 - where the size of the gap is by far less than 0.3µm better than the one shown in Figure 10, where the size of the gap is close to 1.2µm.

In the case of reduction in the time (t=5 sec) in the process of O_2 plasma and the same parameters, we apply the process to Sample 3 and Sample 4 as shown in Figure 11 and Figure 11, where the initial gap size for Sample 3 is 14.5µm whereas after O_2 plasma etching the final of the gap size is 14.7µm and the removal of the resist increases the size of the gap by 0.2µm as shown as in the Figure 10.

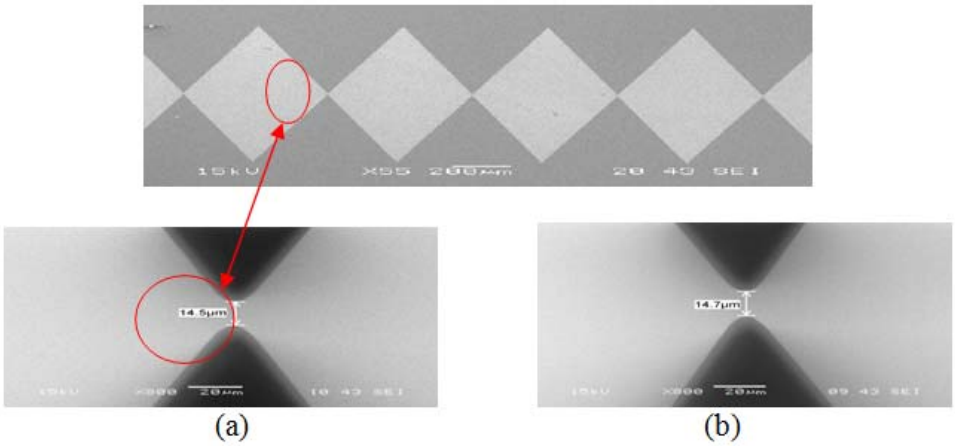

Figure 10: SEM photo show the image gap as 15 kv for sample3:
(a) Before O_2 plasma the size of the gap is 14.5µm, (b) After O_2 plasma the size of the gap is 14.7µm

While in Figure 11 the initial size of the gap for Sample 4 is 3.7µm and after O_2 plasma etching the final gap size is 3.8µm and the resist removal increases the size of the gap by 0.1µm.

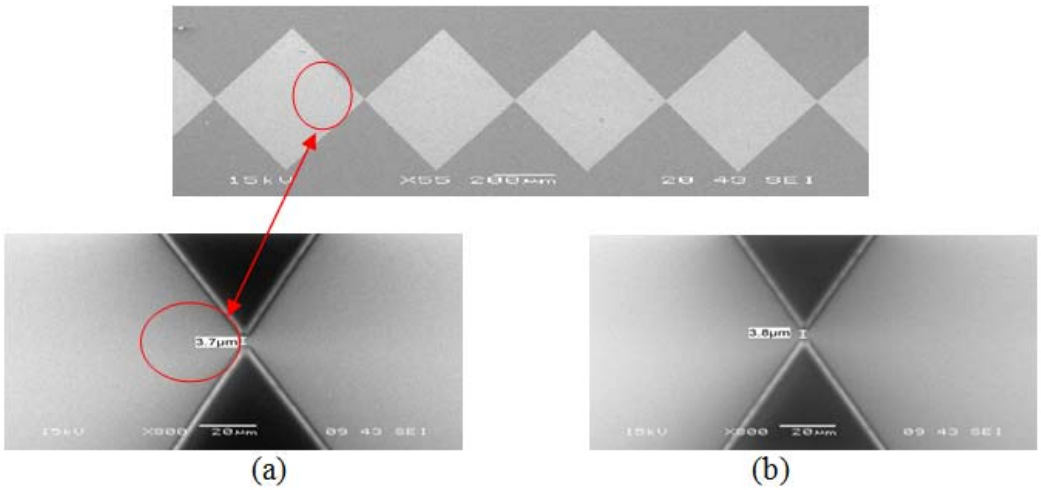

Figure 11: SEM photo show the image gap as 15 kv for sample4:
(a) Before O_2 plasma the size of the gap is 3.7µm, (b) After O_2 plasma the size of the gap is 3.8µm

The amount of etching during the recording of the initial value of the fourth Samples before using the O_2 plasma and then the final value after using the O_2 plasma, and that the time of etching for Sample 1 and Sample 2 is 10 seconds, while for Sample 3 and Sample 4 the etching time is 5sec. Note again that Table 5 shows that the lowest value recorded by the etching results are 0.1µm to a Sample 4 at the time of etching is 5 sec, but the highest rate of etching was recorded for the Sample 2 at 1.2µm when the time of

etching is 10 sec, it is thus clear that the increase in etching time when we apply the O_2 plasma leads to an increase in the amount of etching, while in the case of reducing the time of etching means reducing the amount of etching, as shown in Table 5.

Table 5 : Explain the size gap befor and after apply O_2 plasma process

Sample No.	The size gap before O_2 plasma(μm)	The size gap after O_2 plasma (μm)	Time for O_2 Plasma process
1	7.6	7.9	10 sec
2	6.9	8.1	
3	14.5	14.7	5 sec
4	3.7	3.8	

Compared with Other research has found that in coupled plasma reactive ion etching of SiC single crystals' using NF3-based gas mixtures was investigated [13]. Mesas with smooth surfaces and vertical sidewalls were obtained, with a maximum etch rate of about 400 nm/min. Effects of CH4 and O2 addition to the NF3 gas and the crystalline quality of substrates were studied during the SiC dry etching using various masks. Selectivity of the photoresist (PR) mask improved from about 0.2 to about 0.4 by the addition of 30% CH4 during the RIE, although the etch rate decreased by 50–70% [13]. The first object is to provide the oxygen Reactive Ion Etch (RIE) plasma which contains a sufficient quantity of reducing material to effectively yet safely remove the oxidized organic residues such as oxidized photoresist residues from the semiconductor substrate surfaces

In our limited studies of the effects of PR parameters on O_2 plasma conditions, we have observed that the plasma system is a complex process. By varying a few parameters, we have been able to enhance organic removal rates by several orders of magnitude. We have observed in our laboratory that very small changes in PR parameters can cause large changes in plasma performance.

Discussed in this research are the different parameters used in the process of PR coating and the effect of O_2 plasma process which prepared that the final task is very important in the nanoeletronic fabrication process. the PR here helps as preliminary work on identifying the gap size of the addition to the chrome mask and the specific distinction of the parameters where the results are useful for the O_2 plasma to determine more accurately the breadth of the gap which is less than 0.2μm, and thus presuming the area and prospects for future studies developing Nanotechnology using O_2 plasma technique.

The use of technical O_2 plasma is very useful here in this study and to make the practical Nanogap in the field of Nanoelectronic device fabrication, where after the final use, we need to remove the resist layer to be after the wet etching process to the Al layer, including the use of dry etching by the RIE to the polysilicon layer and then removing the Al layer to be the thin-film deposition of the oxide layer prior to the deposition of Ti/Au, in order to increase connectivity and to facilitate the detection of a

plant's future. After that, the photoresist layer is applied to expose mask2. Then we use the wet etching for Ti/Au layer, after removing the resist, it is the final nanoelectronic device fabrication in this paper as shown in Figure 12.

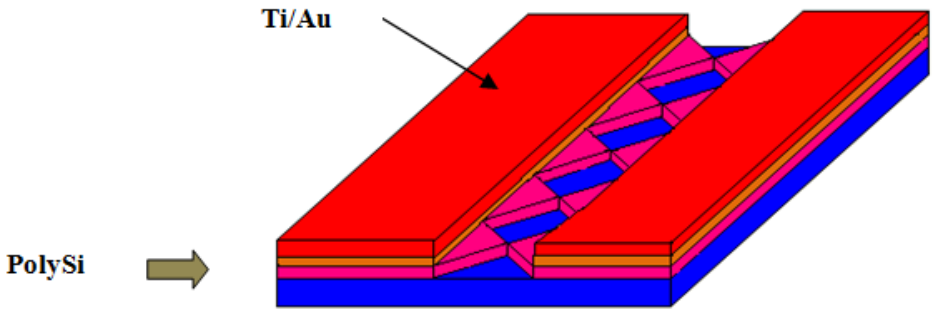

Figure 12: Gold/Ti –Polysilicon/Silicon nano device fabrication

CONCLUSION

These are only a few applications in which an enhanced plasma system may be ideal. Much is known about the optimization of the plasma process, but much more remains to be understood. With a continuing effort to understand the mechanism involve in plasma etching, the usefulness of these systems will expand. Plasma is a viable alternative to other large waste producing techniques; however the slow process time has been the limiting factor in its usefulness. By understanding the mechanism involved in the process of questioning and designing the plasma system to best suit the need, plasma cleaning, etching and machining will become the first choice industrial process.

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